Induction Linac II

9/25/00
S/H

Relevant modifications

1. 2.5 Hz
   6 bunches ~ 20 ms spacing

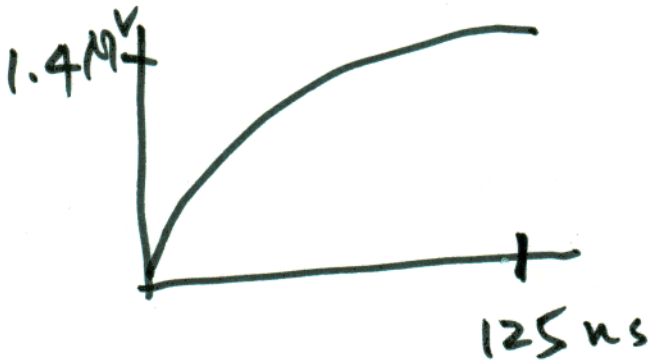
   ⟹ single pulse machine

   ⟹ re-optimization of cores (higher ΔB and/or lower cost material (2605 SC) may be possible

IL 1

100 m

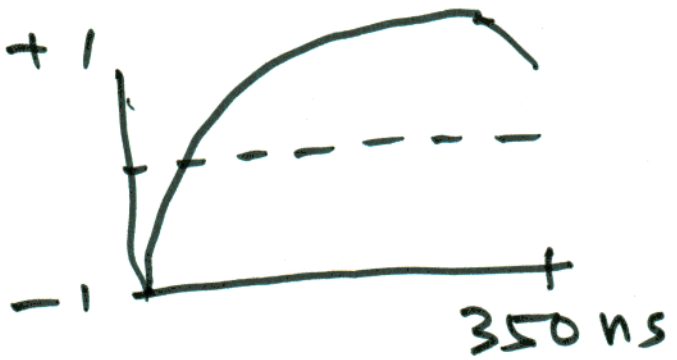
1.4 MV/m



IL 2

80 m

-1.1 to 1.03 MV/m



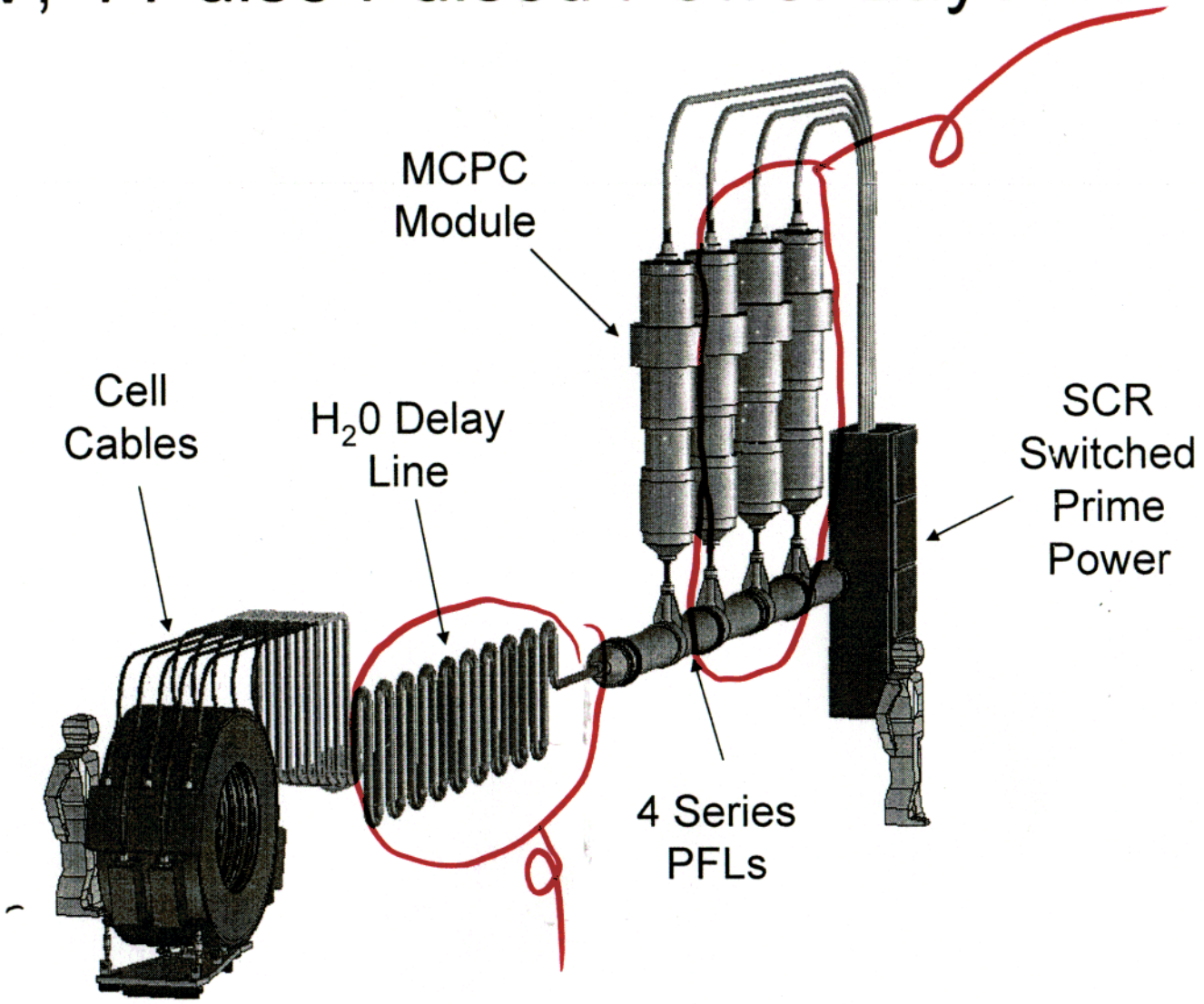
① lower gradient
⇒ better axial packing

② Primarily single polarity
⇒ easier pulser

① longer pulse le
⇒ increased volt-sec
⇒ reduced dB/d
(reduced loss)

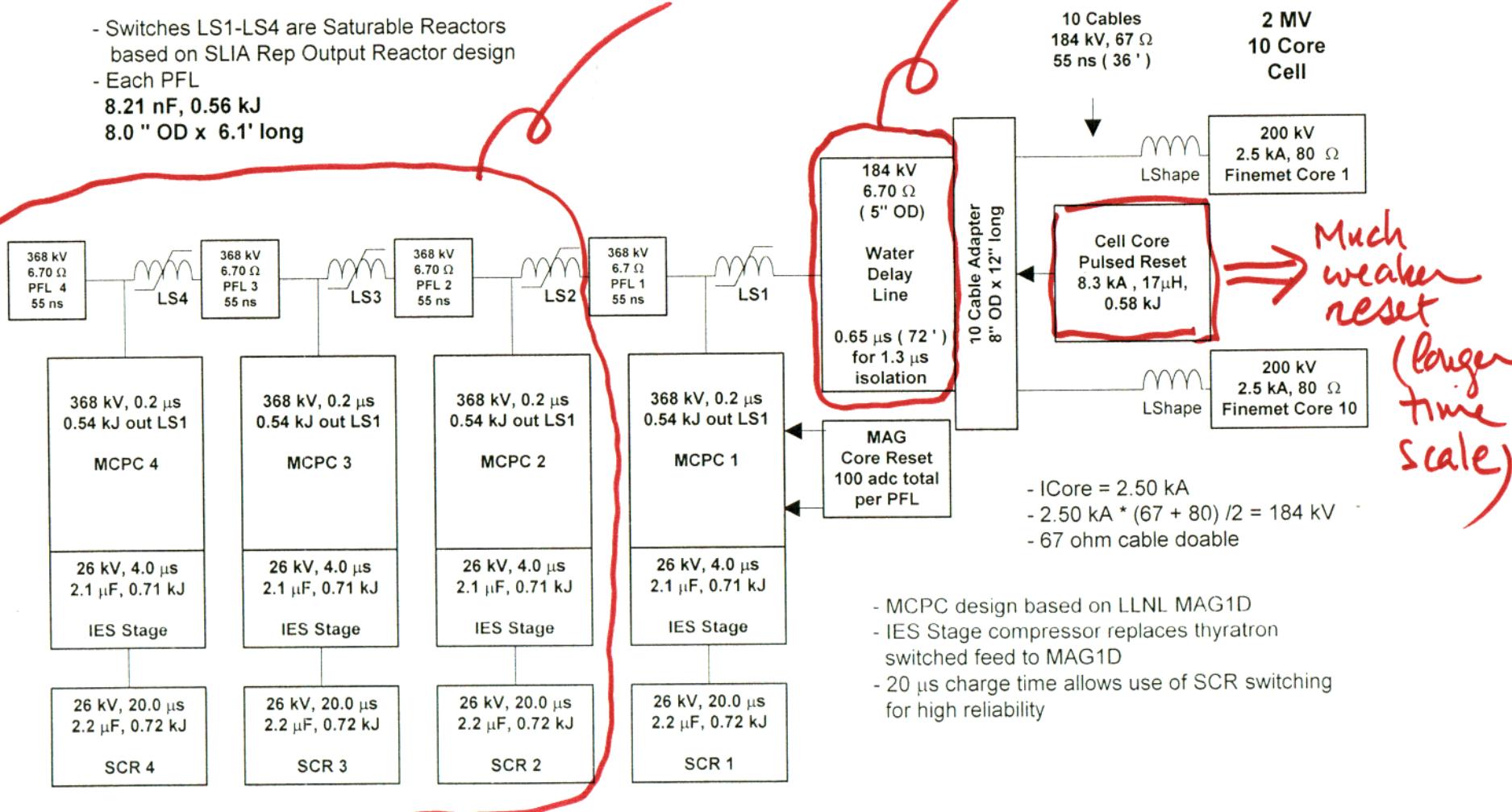
② should revisit optimal architectu
(single pulse) to generate ± polari

2 MV, 4 Pulse Pulsed Power Layout



4 Pulse Pulsed Power System
4 Series PFLs

- Switches LS1-LS4 are Saturable Reactors based on SLIA Rep Output Reactor design
- Each PFL
  8.21 nF, 0.56 kJ
  8.0 " OD x 6.1' long



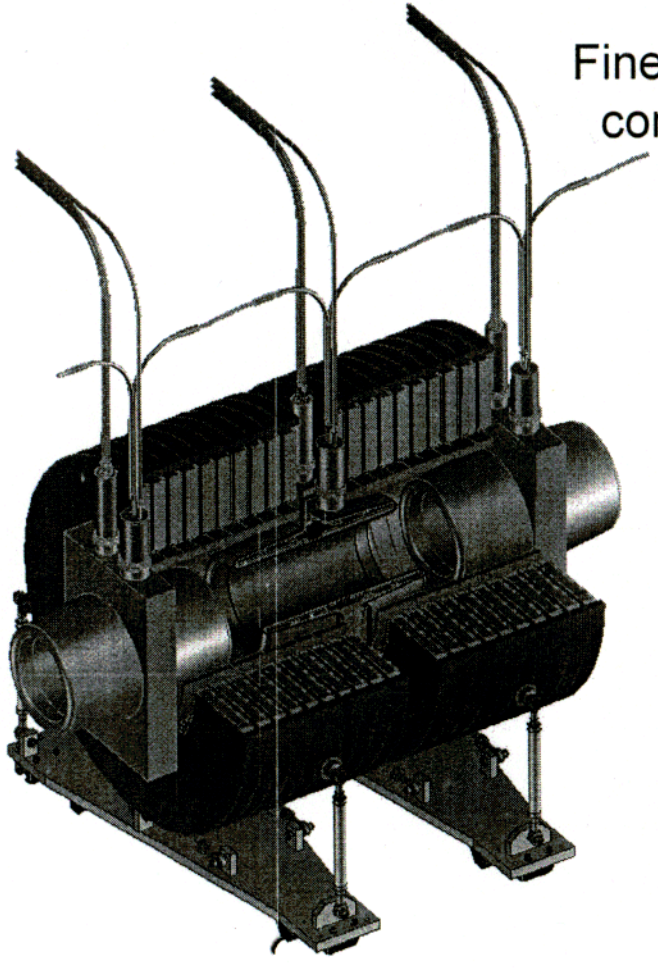
Much weaker reset (longer time scale)

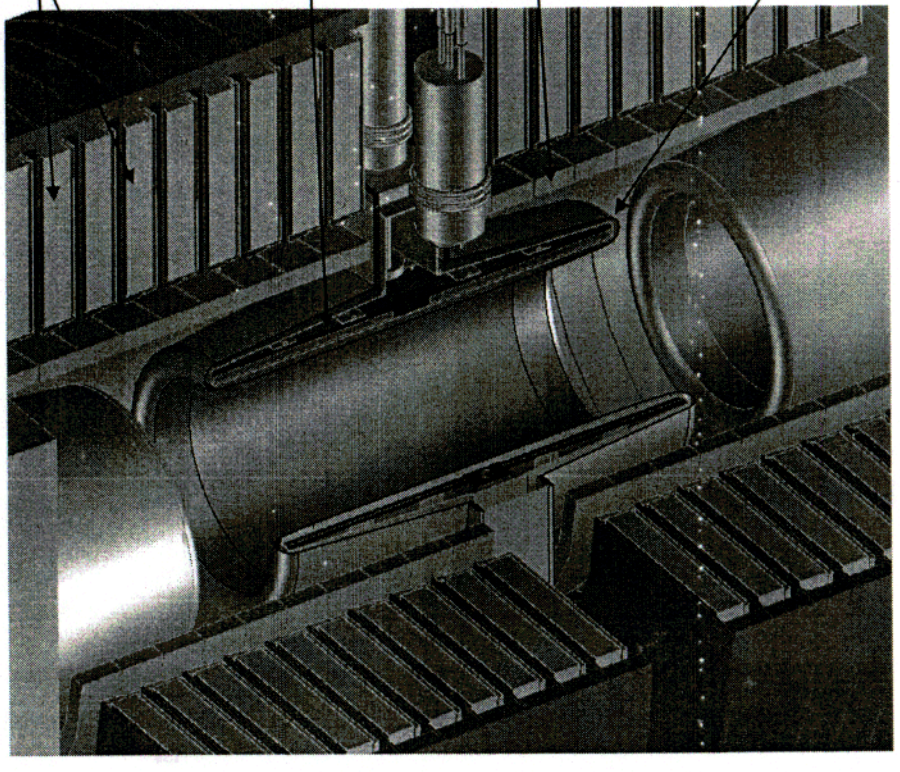
- ICore = 2.50 kA
- 2.50 kA * (67 + 80) /2 = 184 kV
- 67 ohm cable doable

- MCPC design based on LLNL MAG1D
- IES Stage compressor replaces thyratron switched feed to MAG1D
- 20 μs charge time allows use of SCR switching for high reliability

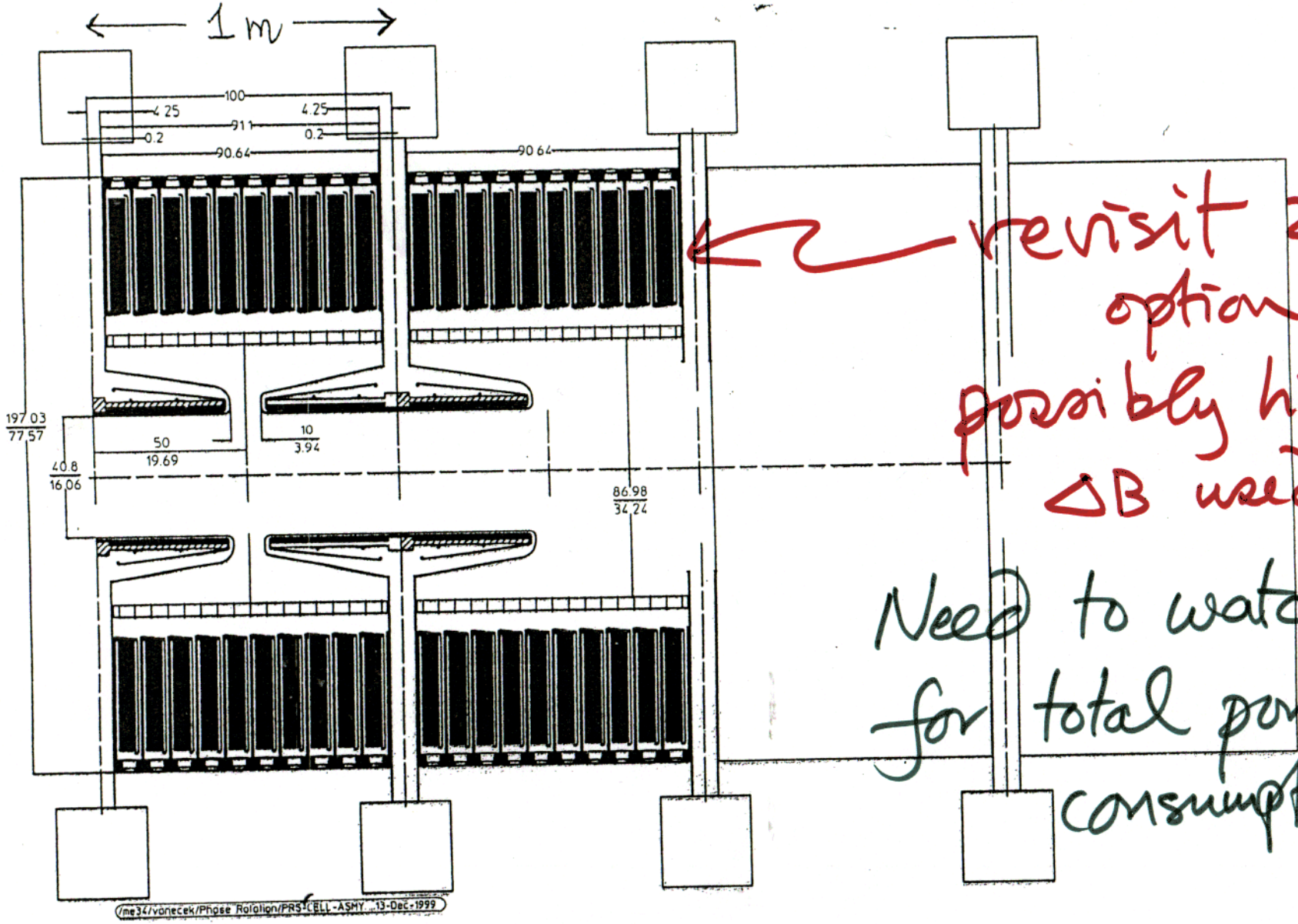
Keep same cell architecture

A Pair of 1 m Long Induction Cells





MUON PHASE ROTATOR



revisit 2605sc option; possibly higher ΔB used

Need to watch out for total power consumption

Re-optimize cell / pulse power balance

Induction Module Core Design

- Requirements => Size
  - 20 cm bore radius & 25 cm for B_Z magnet & Insulator => **Core IR = 45 cm**
  - 90% axial packing & allowable electric field stress => **L = 100 cm**
  - From $V * \tau = \Delta B * A$
    - 2 MV hyperbolic ramp for 100 ns => $V\tau$ = 126 mV-s
    - Balancing pulsed power & core cost => ΔB =1.0 T
    - A = 0.13 m2 , PF_r = 0.70, & PF_a = 0.58 => **Core OR = 78 cm**

ΔV	V_{eff}	τ_r	τ_{flat}	τ_{eff}	$V\tau$	Type	δ	PF_r	ΔB_{max}	Cost	
kV	kV	μs	μs	μs	mV-s	gm/cc			T	Norm	
200	**142**	0.070	0.030	**0.07**	**12.6**	**Finemet**	7.32	0.70	**1.95**	**1.00**	<-- Finemet
200	**142**	0.070	0.030	**0.07**	**12.6**	**2605SC**	7.32	0.70	**2.90**	**0.36**	<-- 2605SC
200	**142**	0.070	0.030	**0.07**	**12.6**	**2605SC**	7.32	0.70	**1.10**	**2.00**	<-- 2714A

ΔB	A_{Met}	A_{Core}	$\Delta B/\Delta t$	L		Δr	r_i	r_o	r_o / r_i	r_{Mean}	H	I_{Core}	E_{core}	k	U_{Met}	V_{Met}	W_{Met}	System $
T	cm^2	cm^2	T/μs	"	cm	cm	cm	cm	cm	cm	kA/m	kA	J	J-μs/T-m^3	J/m^3	cm^3	kgm	Norm
0.97	130	185	**13.2**	2.28	5.8	32.0	45	**77**	1.71	61.0	0.65	**2.50**	31.5	**107**	**634**	49670	363.6	**1.00**
0.82	154	220	11.1	2.28	5.8	37.9	45	**83**	1.84	64.0	0.55	**2.23**	28.1	107	454	61744	452.0	1.02
1.48	85	122	20.1	2.28	5.8	21.0	45	66	1.47	55.5	0.98	3.41	42.9	107	1445	29688	217.3	1.07
0.82	154	220	**11.1**	2.28	5.8	38.0	45	**83**	1.84	64.0	0.98	**3.94**	49.6	**282**	**801**	61946	453.4	**1.13**
2.20	57	82	29.8	2.28	5.8	14.1	45	59	1.31	52.1	2.53	8.28	104.4	282	5571	18736	137.1	2.07
0.82	154	220	**11.1**	2.28	5.8	38.0	45	**83**	1.84	64.0	0.37	**1.50**	18.9	**41**	**306**	61946	453.4	**1.35**
0.86	147	209	11.7	2.28	5.8	36.1	46	82	1.79	64.1	0.39	1.59	20.0	41	339	58981	431.7	1.33

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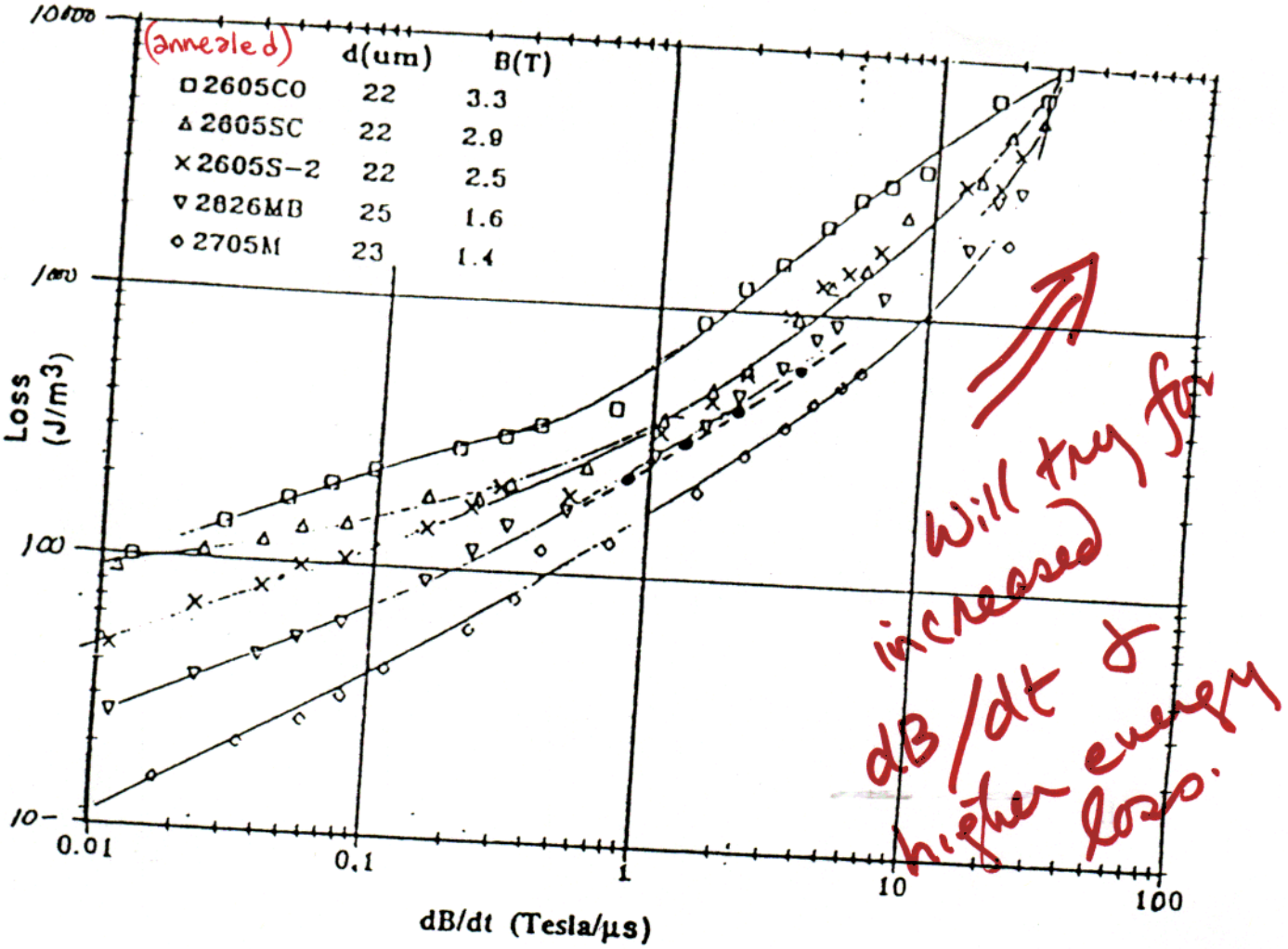

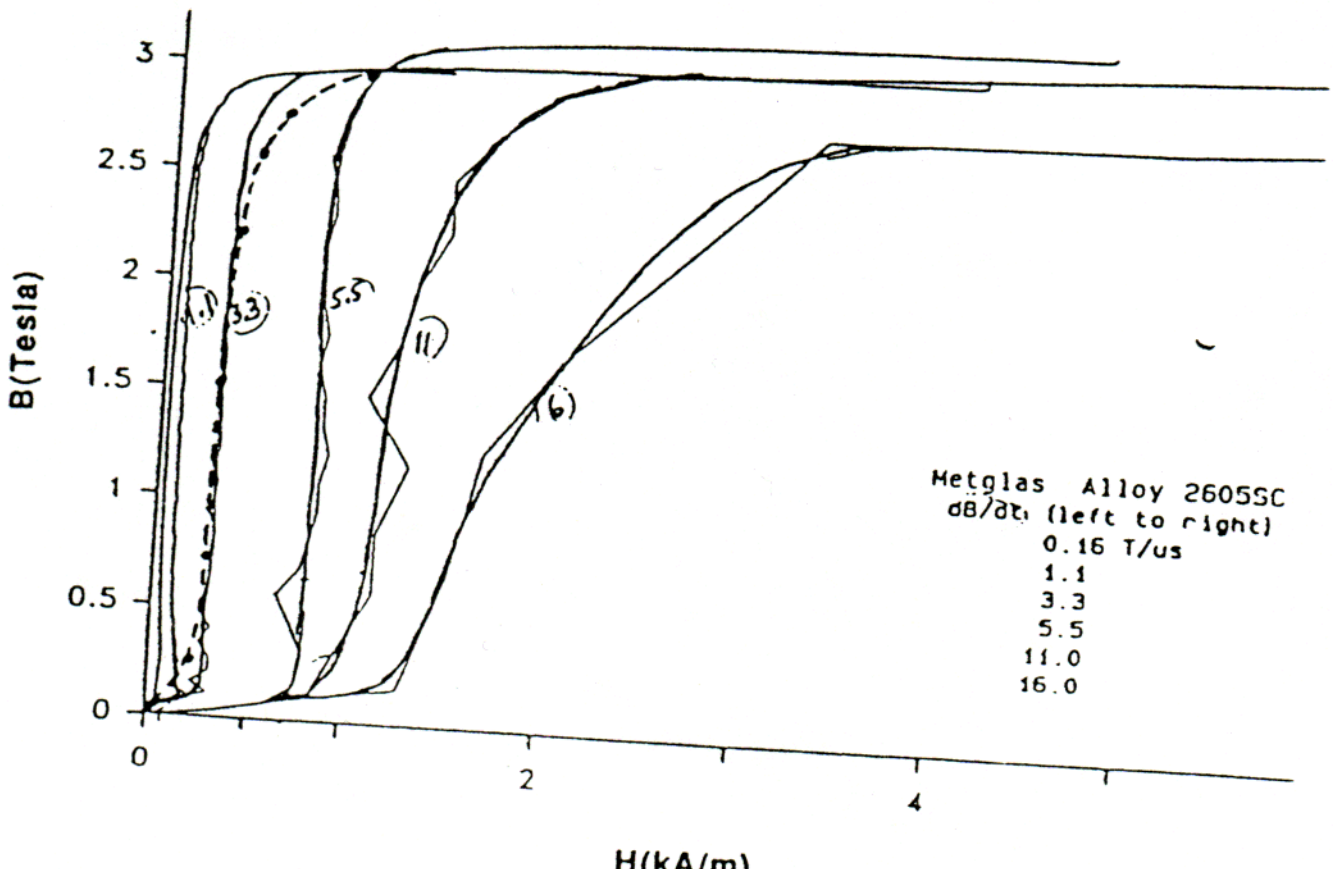

Low level switching should be revisited

SCR Switched Pre-MCPC Power Conditioning

(low rep rate, but 2 frequencies)

- SCR switches are used to ensure reliable
- 6 series 5SGT 40L4502 Gate turn-off Thyristors manufactured by ABB Semiconductors AG
- They discharge a 2.1 μF, 26 kV cap through a 38 μH inductor to feed the 1st stage of the MCPC in 20 μs
- Individual Thyristor parameters are:

	Rating	Used
V (kV)	4.5	4.5
Irms (kA)	2.5	0.3
dI/dt (kA/μs)	0.71	0.71