Induction Linac II

Relevant modifications

1. 2.5 Hz
   6 bunches ~ 20 ms spacing

   \[ \Rightarrow \text{single pulse machine} \]

   \[ \Rightarrow \text{re-optimization of cores (higher DB and/or lower cost material) (2605 SC) may be possible} \]
IL1
100 m
1.4 MV/m

[Graph: 1.4 MV
125 ns]

IL2
80 m
-1.1 to 1.03 MV/m

[Graph: 1
350 ns]

1. Lower gradient
   - better axial packing

2. Primarily single polarity
   - easier pulser

1. Longer pulse length
   - increased volt-sec
   - reduced dB/s
   (reduced loss)

2. Should revisit optimal architecture
   (single pulse) to generate ± polarity
2 MV, 4 Pulse Pulsed Power Layout

MCPC Module

Cell Cables

H₂O Delay Line

4 Series PFLs

SCR Switched Prime Power
4 Pulse Pulsed Power System
4 Series PFLs

- Switches LS1-LS4 are Saturable Reactors based on SLIA Rep Output Reactor design
- Each PFL
  8.21 nF, 0.56 kJ
  8.0" OD x 6.1' long

- MCPC design based on LLNL MAG1D
- IES Stage compressor replaces thyatron switched feed to MAG1D
- 20 μs charge time allows use of SCR switching for high reliability

17-May-00

MuonR&D_Catalina_17May00.ppt
Keep same cell architecture

A Pair of 1 m Long Induction Cells

Finemet cores  Superconducting Solenoid  Mycalex Insulator  Induction Gap
MLON PHASE ROTATOR

- Revisit 260550 option; possibly higher DB used
- Need to watch out for total power consumption
Re-optimize cell / pulse power balance

Induction Module Core Design

- Requirements => Size
  - 20 cm bore radius & 25 cm for $B_z$ magnet & Insulator => Core IR = 45 cm
  - 90% axial packing & allowable electric field stress => $L = 100$ cm
  - From $V \times \tau = \Delta B \times A$
    - 2 MV hyperbolic ramp for 100 ns => $V\tau = 126$ mV-s
    - Balancing pulsed power & core cost => $\Delta B = 1.0$ T
    - $A = 0.13$ m², PF$_r = 0.70$, & PF$_a = 0.58$ => Core OR = 78 cm

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<th>$\Delta V$</th>
<th>$V_{eff}$</th>
<th>$\tau_r$</th>
<th>$\tau_{flat}$</th>
<th>$\tau_{eff}$</th>
<th>$V\tau$</th>
<th>Type</th>
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System $\Delta B$

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<th>$A_{Core}$</th>
<th>$\Delta B/\Delta t$</th>
<th>$L$</th>
<th>$\Delta r$</th>
<th>$r_i$</th>
<th>$r_o$</th>
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<th>$H$</th>
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<th>$E_{Core}$</th>
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Low level switching should be revisited

SCR Switched Pre-MCPC Power Conditioning

- SCR switches are used to ensure reliable
- 6 series 5SGT 40L4502 Gate turn-off Thyristors manufactured by ABB Semiconductors AG
- They discharge a 2.1 μF, 26 kV cap through a 38 μH inductor to feed the 1st stage of the MCPC in 20 μs
- Individual Thyristor parameters are:

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<th>Rating</th>
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<td>Irms (kA)</td>
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